REMARKS

Claims 1-7 and 16-20 are pending in the application. Claims 1 and 16 have been amended by this paper. No claims have been cancelled by this paper. No new matter has been added. The Applicant requests consideration of the following Remarks and allowance of the claims.

Claim rejections -- 35 USC §103

Claims 1-7, and 16-20 were rejected under 35 USC 103(a) as being unpatentable over Paul (US 6,466,972) in view of Wisor (US 6,021,498). Claims 2-7 and 17-20 were rejected under 35 USC 103(a) as being unpatentable over Paul (US 6,466,972) in view of Wisor (US 6,021,498) and Spencer (US 6,021,498). Applicant respectfully traverses the rejection for at least the following reasons.

The Examiner asserts that Paul discloses (1) a device hardware abstraction layer adapted to configure multiple instantiations, and (2) a platform hardware abstraction software layer adapted to configure each instantiation of the peripheral device via calls to the device hardware abstraction layer. Wiser, the Examiner asserts, discloses defining offset values for registers and defining a data structure for the peripheral device.

Wiser discloses a program register and an index register where the value in the index register determines which peripheral register is written/read during an I/O cycle. Thus, Wiser discloses a hardware indirect pointer register. Because it is a register, it is a purely hardware concept. Applicant's amended claims call for the *offset values for registers* to be defined *relative to a variable base address received as a parameter passed to the device hardware abstraction software layer*. Applicant's amended claims also call for the structure to access *the registers of the peripheral device relative to the variable base address*. Thus, Applicant's claims call for "parameters" (i.e., arguments passed to a subroutine). Furthermore, Applicant's amended claims specify how the *base address* is received—*as a parameter*. Wiser receives the value for the pointer register via an I/O

write—which is hardware signaling across a bus. See Wiser Column 4, lines 36-38. Thus, Wiser does not disclose passing the base address of a peripheral to a subroutine.

Furthermore, the hardware pointer of Wiser does not *define* a *data structure* that accesses *the registers of the peripheral device relative to the variable base address.* The hardware pointer of Wiser arguably defines the base address. However, it does not define for other pieces of software, and the *platform hardware abstraction layer* in particular, which offsets from that base address are valid and may be used to access the registers of the peripheral. Thus, the hardware pointer of Wiser does not *define* a *data structure* that accesses *the registers of the peripheral device relative to the variable base address* within the meaning of Applicant's independent claims.

Accordingly, Applicant respectfully submits that all of the limitations, in Applicant's independent claims 1 and 16, are not disclosed, taught or suggested by the prior art. "To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." See In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All of the claim limitations must be "considered" by the Examiner. See MPEP 2143.03. Applicant respectfully submits that independent claims 1 and 16 are therefore patentable over Paul and Wiser.

The dependent claims, while separately allowable over the art of record, depend from otherwise allowable independent claims. The Applicant therefore refrains from a discussion of the dependent claims for the sake of brevity.

Please note that claim 1 was amended to address an antecedent basis issue.

For these reasons, this application is now considered to be in condition for allowance, and such action is earnestly solicited.

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Respectfully submitted

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